IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
PIO

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **ELECTRONIC MEMORY CIRCUIT AND RELATED MANUFACTURING METHOD**

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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification to label FIGS. 1-5 prior art and to add a reference numeral to FIG. 6 as indicated in red ink.

In the Claims:

Please cancel Claims 1-7.

Please add new Claims 8-25.

8. A method for manufacturing an EEPROM comprising a matrix of memory cells arranged in pairs, the method comprising:

forming active areas in a substrate;

forming doped regions in the substrate;

forming layers of oxide of different thicknesses on the substrate;

forming a common source region for each pair of memory cells;

selectively forming a first layer of polysilicon;

selectively removing the first layer of polysilicon from the common source region;

forming an intermediate dielectric layer; and

forming a second layer of polysilicon to form a common control gate region for pairs of the memory cells having a common source region.

9. A method according to Claim 8 wherein the pairs of memory cells having the common source region belong to a same byte.

10. A method according to Claim 9 wherein the common control gate regions of the pairs of memory cells belonging to the same byte are connected to a common control gate line.

11. A method according to Claim 10 further comprising forming an enabling transistor to address the common control gate line.

12. A method according to Claim 11 wherein the enabling transistor comprises a MOS transistor.

13. A method according to Claim 8 wherein the common control gate region overlies the common source region.

14. A method according to Claim 8 wherein the memory cells of each pair of memory cells are arranged symmetrically with respect to the common source region.

15. A method for manufacturing a pair of memory cells for an EEPROM including a matrix memory cells, the method comprising:

forming active areas in a substrate for each memory cell;

forming respective drain regions in the substrate for each memory cell;

forming layers of oxide of different thicknesses adjacent the substrate;

forming a common source region in the substrate for the pair of memory cells;

selectively forming a first layer of polysilicon over the substrate;

selectively removing a portion of the first layer of polysilicon from the common source region;

forming an intermediate dielectric layer over the first layer of polysilicon; and

forming a second layer of polysilicon over the intermediate dielectric layer to form a common control gate region for the pair of memory cells.

16. A method according to Claim 15 wherein the common control gate region overlies the common source region.

17. A method according to Claim 15 wherein the memory cells of each pair of memory cells are arranged symmetrically with respect to the common source region.

18. A method of making a memory circuit comprising:

forming a plurality of rows and columns of EEPROM memory cells, each memory cell including a MOS floating gate transistor and a selection transistor; and

symmetrically arranging the memory cells in pairs with a common source region and a common control gate region.

19. A method according to Claim 18 wherein each row of memory cells comprises a word line and each column of memory cells comprises a bit line organized in line groups to group the memory cells in bytes, each of which has an associated control gate line.

20. A method according to Claim 19 wherein the pairs of memory cells having the common source region belong to a same byte.

21. A method according to Claim 20 wherein the common control gate regions of the pairs of memory cells belonging to the same byte are connected to a common control gate line.

22. A method according to Claim 21 further comprising the step of forming an enabling transistor to address the common control gate line.

23. A method according to Claim 22 wherein the enabling transistor is a MOS transistor.

24. A method according to Claim 18 wherein the common control gate region overlies the common source region.

25. A method according to Claim 18 wherein the memory cells of each pair of memory cells are arranged symmetrically with respect to the common source region.

REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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